High Performance Baugh Wooley Multiplier using Carry Skip Adder Structure

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Abstract—The Baugh-Wooley algorithm is a fine iterative algorithm for performing multiplication in digital signal processing typed applications. Decomposition sense is used with Baugh-Wooley algorithm to enhance the speed and to reduce the critical path delay. In this thesis a high speed multiplier is designed and implemented using decomposition logic and Baugh-Wooley algorithm. The outcome is compare with booth multiplier. FPGA based architecture is presented and design has been implemented using Xilinx 12.3 device. The modified-Booth algorithm is extensively used for high-speed multiplier circuits. In designs based on reduction trees with logarithmic logic depth, however, the reduced number of partial products has a imperfect impact on overall performance. The Baugh-Wooley algorithm is a different scheme for signed multiplication, but is not so widely adopted because it may be difficult to deploy on irregular reduction trees. We apply the Baugh-Wooley algorithm in an High Performance Multiplier (HPM) tree, which combines a regular layout with a logarithmic logic depth. We show for a range of worker bitwidths that, when implemented in 130-nm and 65-nm process technologies, the Baugh-Wooley multipliers exhibit similar delay, less power dissipation and smaller area foot-print than modified-Booth multipliers.

Keywords— Carry skip adder (CSKA), energy efficient, high performance, hybrid variable latency adders, Wallace Tree Multiplier.

1. INTRODUCTION

Multipliers play a vital role in various high performance systems such as Microprocessor, FIR filters, Digital Processors, etc. Multipliers are a crucial part of the modern electronic era. Multipliers can found electronics systems that run compound calculations especially in DSP processor, Microcontroller and Microprocessor. Many transform algorithms like Fast Fourier transforms (FFTs), DFT etc make use of various multipliers. Multiplication is an important arithmetic operation and multiplier implementations date a number of decades back in time. Multiplications were originally performed by iteratively utilizing the ALU’s adder. As time constraints became stricter with increasing clock rates, keen multiplier hardware implementations such as the array multiplier were introduced. Low power adder circuits have become very important in VLSI industry. Adder circuit is one of the important building blocks in DSP processor. Adder is the main component in most of the arithmetic unit. Adders plays important component in digital systems because of the more number for use in other essential digital operations such as subtraction, multiplication and division. Hence, the improving performance of the digital adder increase the execution of various binary operations in a circuit consisting of different blocks. There are many plant on the subject of optimizing the speed and power of these units, which has been reported in [2]-[9]. Obviously, it is extremely possible to achieve top speeds at low-power and energy consumptions, which is one of the challenges for the designers of general purpose processors

2. LITERATURE REVIEW

Milad Bahadori, Mehdi Kamal and et al., (2015) have dealt with the High-Speed and Energy-Efficient Carry Skip Adder Operating Under A Wide Range of Supply Voltage Levels. Carry skip adder (CSKA) structure that has a higher speed yet lower energy consumption compared with the conventional one. The speed enhancement is achieved by applying concatenation and incrementation schemes to improve the efficiency of the conventional CSKA (Conventional-CSKA) structure. A hybrid variable latency extension of the proposed structure, which lowers the power consumption without considerably impacting the speed, is presented. R.Zlatanovici, S.Kao, and et al., (2009) have implemented the Energy-Delay Optimization of 64-Bit Carry-Look ahead Adders With a 240 ps 90 nm CMOS Design Example. The methodology for energy-delay optimization of digital circuits is presented. This methodology is applied to minimizing the delay of representative carry look ahead adders under energy constraints. Impact of various design choices, including the carry look ahead tree structure and logic style, are analyzed in the energy–delay space and verified through optimization.

S. K. Mathew, M. A. Anders, and et al., (2005) have implemented a 4-GHz 300-mW 64-bit integer execution ALU with dual supply voltages in 90-nm CMOS. A 64b integer execution ALU is described for 4GHZ single cycle operation with a 32b mode ALU latency of 7 GHZ. The 0.073 mm² chip is fabricated in a 90nm dual-v, CMOS technology and dissipates 300Mw. sparse-tree adder structure, single rail dynamic circuits, and a semi dynamic implementation enables a 20 % performance improvement and a 56% energy reduction. Vojin G. Oklobdzija and et al., (2005) have analyzed the Comparison of High-Performance VLSI Adders in the Energy-Delay Space. We motivate the concept of comparing very large scale integration adders based on their energy-delay characteristics and present results of our estimation technique. This stems from a need to make appropriate selection at the beginning of the design process. The estimation is quick, not requiring extensive simulation or use of computer-aided design tools, yet
sufficiently accurate to provide guidance through various choices in the design process. B. Ramkumar and Harish M Kittur (2012) have dealt with the Low-Power and Area-Efficient Carry Select Adder. Carry Select Adder (CSLA) is one of the fastest adders used in many data-processing processors to perform fast arithmetic functions. From the structure of the CSLA, it is clear that there is scope for reducing the area and power consumption in the CSLA. This work uses a simple and efficient gate-level modification to significantly reduce the area and power of the CSLA.

M. Vratonjic, B. R. Zeydel, and et al., (2005) have implemented a Low and ultra low-power arithmetic units: Design and comparison. The design guidelines for low and ultra low power units are presented. Based on this modification 8-, 16-, 32-, and 64-b square-root CSLA (SQRTCSLA) architecture have been developed and compared with the regular SQRT CSLA architecture. We analyze the structure for addition in energy delay scale optimization. C. Nagendra, M. J. Irwin, and et al., (1996) have analyzed a Area-time-power tradeoffs in parallel adder. The several classes of parallel, synchronous adders are surveyed based on their power, delay and area characteristic. The adders studied include the linear time ripple carry and Manchester carry chain adders. The most of the research is last few decades has concentrated on reducing the delay of addition. D. Markovic, C. C. Wang and et al., (2010) have implemented the Ultralow-power design in near-threshold region. The operation in the sub threshold region most often is synonymous to minimum energy operation. An energy delay modeling framework that extends over a weak, moderate and strong inversion region is developed. This operation from a need to make appropriate selection at the beginning of the design process.

Y.Chen, H. Li, J. Li, and et al., (2007) have dealt with the Variable-latency adder(VL-adder): New arithmetic circuit design practice to overcome NBTI. Negative bias temperature instability (NBTI) has become a dominant reliability concern for nanoscale PMOS transistors. We propose variable latency adder technique for NBTI tolerance. By detecting the circuit failure on the fly, the proposed VL adder can automatically shift data capturing clock edge to tolerate NBTI-induced delay degradation on critical timing paths. S. Ghosh and K. Roy (2008) have implemented the Exploring high-speed low-power hybrid arithmetic units at scaled supply and adaptive clock-stretching. Meeting power and performance requirement is a challenging task in high speed ALUs. Supply voltage scaling is promising because it reduces both switching and power but it also degrades robustness. The idea is based on the fact that the critical paths of arithmetic the supply voltage to operate non critical paths at rated frequency and delay failure in the critical path.Y. Chen et al., (2010) have analyzed the Variable-latency adder (VL-adder) designs for low power and NBTI tolerance. We have proposed a new adder design called variable-latency adder (VL-adder). This technique allows the adder to work at a lower supply voltage than that required by a conventional adder while maintaining the same throughput.

The VL-adder design can be further modified to overcome the effects of negative bias temperature instability (NBTI) on circuit delay. By applying VL-adder concept to a 64-bit carry select adder design, more than 40% energy saving is obtained when a similar throughput is maintained.

3.BAUGH-WOOLEY MULTIPLIER

In signed multiplication the duration of the partial products and the number of partial products will be very high. So an algorithm was introduced for sign multiplication called as Baugh Wooley algorithm. The Baugh-Wooley multiplication is one amongst the cost-effective ways to hold the sign bits. This method has been developed so as to style regular multipliers, suited to 2's compliment numbers. Baugh-Wooley multiplier hardware architecture is shown in figure 1. It follow left shift algorithm. Mux can choose which bit will multiply. Suppose we multiply +4 and -4 in decimal we get '0'. Now, after representing these numbers in two’s compliment form we get +4 as 0100 and -4 as 1100. On adding these two binary numbers we get 10000. Discard carries, then number is represented as '0'.

![Figure 3.1 Hardware implementation of Baugh-Wooley Multiplier](image)

As shown in Figure 3.1 Baugh-Wooley Multiplier provides a high speed, signed multiplication algorithm [5]. It uses similar products to complement multiplication and adjusts the partial products to maximize the regularity of multiplication array [6]. When digit is represented in two’s compliment form, sign of the number is embedded in Baugh-Wooley multiplier.

4. BAUGH-WOOLEY MULTIPLICATION

Baugh-Wooley schemes become an area strong when operands are greater than or equal to 32 bits. The reason for using triangular shaped is that the triangular cell position in the reduction tree technique has a shorter wire length. In the paper aim and implementation of conventional 8 bit Baugh Wooley multiplier algorithm has done and compared the result obtained with the new drawing of 8 bit Baugh Wooley multiplier algorithm using HPM reduction tree [6].

The comparative study has been done to prove that the new Baugh Wooley multiplier design is faster than the conventional design. The algorithm for Baugh Wooley multiplier is shown Figure 4.1.
5. RESULT AND DISCUSSION

The design planned in this paper has been developed using MODEL SIMULATOR. Decomposition logic is implemented with Baugh-Wooley multiplier which shows the improved results in terms of path delay and speed. The design operates on maximum frequency of 95.9MHz. The considerable raise in speed make the design suitable for many high performance system such as Digital Signal Processors, FIR filters, Microprocessors etc. When multiplying twos compliment numbers directly, each of the part products to be added is a signed numbers. Thus all partial product has to be sign extended to the width of the final product in order to form a correct sum by the Carry Skip Adder (CSA) tree.

6. CONCLUSION

Multipliers are a crucial part of the modern electronic era. Multipliers can found electronics systems that run compound calculations especially in DSP processor, Microcontroller and Microprocessor. Many transform algorithms like Fast Fourier transforms (FFTs), DFT etc make use of various multipliers The carry skip adder structure is applied to an Baugh Wooley Multiplier where the structure is performed in parallel manner and the power consumption is reduced and because of parallel operation the power consumption and the area is reduced. The reduction in area in terms reduces the complexity of the structure.

REFERENCES