DESIGN OF VARIABLE LATENCY BY PASS MULTIPLIER WITH ADAPTIVE HOLD LOGIC

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Abstract—Multiplication is important in arithmetic operations such as fourier transform, microprocessors, etc. System performance is based on the multiplier throughput. Pmos transistor and Nmos transistor is affected by temperature instability. It affects the system performance. so it is necessary to design multiplier with reliability. In this the multiplier is designed with flipflop and AHL circuit. The number of clock cycle is high in fixed latency. In Variable latency the number of clock cycle is reduced. More number of zeros is inserted in the column by pass method so this reduces the switching activity. Hence the power consumption is reduced. In this paper variable latency column by pass multiplier is designed to reduce the timing wastage, performance degradation and to increase the speed of the circuit.

Keywords—multiplier, flipflop, AHL circuit, variable latency.

1. INTRODUCTION

Multipliers are important in high performance systems. The performance of the system will be decreased if the multiplier is slow. An integer is added specified number of times in multiplication. M partial products are together added by the shift and add multiplication algorithm. Partial product is obtained by multiplying the multiplier bit with the multiplicand bit. Binary multiplication is simpler than decimal multiplication. Negative bias temperature instability effect affects the CMOS technology when it is scaled down. CMOS transistor is scaled down to ultra deep submicron technology die temperature becomes higher due to NBTI impact. Device aging process i.e. negative bias temperature instability effect affects the circuit performance. NBTI effect is generated at si interface at pmos transistor under negative bias. Due to the interaction of inversion layer holes and hydrogen passivated si atom the si-H bond is broken. This bond is generator during oxidation process it generates H molecule. Interface traps are generated when these molecules diffuse. Interface traps are accumulated between gate oxide interface and silicon as a result threshold voltage is increased and the switching speed of the circuit is reduced. Therefore it is important to design a high performance reliable multiplier. In pmos transistors two phase of NBTI effects are considered based on bias condition. In the first phase when the gate voltage is zero i.e (Vg=0) H atoms diffuses towards the gate and positive traps are accumulated during stress time. This phase is called stress NBTI. In the second phase gate voltage is equal to VDD i.e. Vg=VDD new traps are not generated and the H atom diffuses. The broken si-H is annealed by H atoms. In this stage the number of interface traps are reduced. This phase is called recovery. When nmos transistor is in positive bias, positive bias temperature instability occurs[3]. PBTI effect is smaller than the NBTI effect therefore it is ignored.

In traditional method guard-bandning and gate oversizing are used to reduce the aging effect but area and power are inefficient in this approach. NBTI methodologies are used to mitigate this problem. Wu and Diana Marculescu proposed [6] the pin reordering and logic restructuring framework to mitigate the performance degradation caused by NBTI effect. This framework is based on wire reconnection it does not involves gates or transistors. Switching activity is reduced by wire reconnection. They also proposed an aging-aware optimization and timing analysis [7] by using path sensitization.

As the scale of integration keeps growing, more and more sophisticated signal processing systems are being implemented on a VLSI chip. These signal processing applications not only demand great computation capacity but also consume considerable amount of energy. The need for low-power VLSI system arises from two main forces. First, with the steady growth of operating frequency and processing capacity per chip, large currents have to be delivered and the heat due to large power consumption must be removed by proper cooling techniques. Second, battery life in portable electronic devices is limited. Low power design directly leads to prolonged operation time in these portable devices. The multiplier is fairly large block of a computing system. The size of multiplier is directly proportional to the square of its resolution i.e. size of multiplier.

Yu-Hung cho and Yi-Ming Yung proposed a general model to mitigate performance degradation that is due to the aging effect. This model propose an aging-aware multiplier design with a novel adaptive hold logic (AHL) circuit. The multiplier is able to provide higher throughput through the variable latency and can adjust the AHL circuit to mitigate performance degradation that is due to the aging effect. Moreover, the proposed architecture can be applied to a column- or row-bypassing multiplier.

2. RELATED WORK

A. Row-Bypassing Multiplier

In the row-by-passing multiplier some rows or columns of the multiplier are turned off in the multiplier array when the multiplier bits are zero. The activity power of the array multiplier is reduced by the row-by-passing
multiplier. During the operation of the multiplier some adder rows are disabled to save power.

B. Column-Bypassing Multiplier

In the column by passing multiplier Fig.1, a column is disabled when the corresponding multiplier bit is zero. Columnbypassing technique depends on the zeros in the multiplicand bit.

This multiplier consists of carry save adder. Each carry save adder has fulladder cells. The output of the fulladder is sum bit and carry bit. The output of the sum bit goes down and the output of the carry bit goes to the lower left of the full adder. For the carry propagation ripple adder is in the last row.

c. Fixed latency

Fixed latency multiplier takes 32 cycles. If the LSB bit of the b operand is zero then b operand is shifted to the right and a operand is shifted to the left. If the LSB bit is one then a is added to the result before shifting. Each iteration calculates the partial product of the multiplication. An alternative approach to fixed latency multiplier is variable latency multiplier.

3. LATENCY ARCHITECTURE

The proposed multiplier Fig.2 has razor flip-flops, multiplier, and adaptive hold logic circuit. This architecture has two m-bit inputs and one 2m-bit output. Depending on the number of zeros in the multiplicand bit the multiplier is examined. It is examined to determine whether the operation requires one clock cycle or two clock cycle. In random input pattern zeros and ones in the multiplicand and multiplier follows normal distribution.

4. RAZOR FLIP FLOP

Razor flip flop determines the timing violations in the input pattern. Razor flip flop consists of main flip flop, XOR gate, shadow latch, and MUX. Main flip flop is used to catch a normal clock signal. Shadow latch is used to catch a delayed clock signal. If the main flip flop bit and the latched shadow latch bit is different then the result is incorrect. The error signal is set to 1 and operation is reexecuted.

5. ADAPTIVE HOLD LOGIC

In variable latency multiplier design the main component is the adaptive hold logic. It contains aging indicator, D flip flop, MUX and judging block. Aging indicator is used to determine the performance degradation of the system. Counter is implemented as an aging indicator. The number of errors in certain operation is counted by the simple counter and it is reset to zero at the end of operation.

6. VARIABLE LATENCY DESIGN

Variable latency is used to reduce the timing wastage in the circuit. In this longer paths are executed using two cycles and
shorter paths are executed using shorter cycle. Average latency is smaller in the variable latency design.

The 8-bit ripple carry adder with a hold logic circuit. It has 8-bit input and output. Maximum delay for the adder is 8 if the delay for the full adder is one. In column by passing multiplier operation path delay is connected to the zeros in the multiplicand bit. When number of zero is increased then the average delay is reduced and delay distribution is shifted to the left. In column by passing multiplier multiplicand is used as the select line and in row by passing multiplier multiplicator is used as the select line.

7. RESULT ANALYSIS

The results are obtained for the fixed latency and variable latency column and row by pass multiplier. The codings are developed for 4-bit, 16-bit and 32-bit variable latency and fixed latency column by pass multiplier using VHDL language and are simulated on modelsim software. Then it is implemented in FPGA.

<table>
<thead>
<tr>
<th>FLCB</th>
<th>VLCB</th>
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<tbody>
<tr>
<td>COLUMN</td>
<td>COLUMN</td>
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<td>Area</td>
<td>Delay</td>
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<tr>
<td>590</td>
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8. CONCLUSION

In this project the column and row by passing array multiplier have been studied and also the impacts of area, delay and power have been analyzed. Simulation results have been calculated. As compared with the existing architecture Wallace tree based multiplier increases speed and reduces area, then reduces the performance degradation. Then the technique is implemented in Spartan 3E.

REFERENCES

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