DESIGN OF CONSTANT MULTIPLIER ARCHITECTURE FOR FIR FILTER BASED ON SUB-SUBTRACTION ALGORITHM

Divya.P¹, Valluvan.K.R²

¹(Department of ECE, PG student, Velalar College of Engineering & Tech., Thindal, Erode, India, divyapmece@gmail.com)
²(Department of ECE, Professor & Head, Velalar College of Engineering & Tech., Thindal, Erode, India, krvalluvan@gmail.com)

Abstract—FIR filter has wide application as a component in any digital signal processing, image and video processing, wireless communication and biomedical signal processing systems. Significant applicability of an efficient reconfigurable FIR filter motivates the system designer to develop the chip with low cost, power, and area along with the capability to operate at very high speed. In existing methods, an efficient fixed point reconfigurable FIR filter is implemented using Vertical-horizontal Binary Common Sub-expression Elimination (VHBCSE) algorithm. The area and power are increased by the use of adders. In the proposed method, subtractor will be used instead of adders. The design is coded in Very High Speed Integrated circuit Hardware Description Language (VHDL) and simulated in ModelSim and synthesized in Electronic Design Automation (EDA) tool Xilinx ISE 9.2i. The subtractor is proposed by sub-subtraction algorithm and its area, delay and power be compared with that of the existing method.

Keywords—FIR filter, VHBCSE, Fixed point reconfigurable FIR filter, sub-subtraction algorithm

1. INTRODUCTION

The demand for digital signal processing (DSP) systems with low power are increasing due to explosive growth in portable multimedia applications and mobile computing. Most of the DSP operations are performed by Finite impulse response (FIR) filtering. FIR digital filters are widely used in any digital signal processing, image and video processing, biomedical signal processing, and wireless communication systems. Generally, FIR filter structures are implemented by using add and shift operations.

The multiplication of input samples with filter coefficients dominates the complexity of a FIR filter. Constant multiplication scheme will reduce the number of adders and subtractors used in the FIR filters. In multiple constant multiplications (MCM), the multiplication operation can be performed by one particular variable (the input) and many constants (the coefficients).

MCM is used to produce constant multiplication in multiple input multiple output (MIMO) systems, DSP systems, frequency multiplications, error correcting codes, graphics and control applications. For those applications full fledged multipliers are not needed. Constant coefficients are used to produce constant multiplication.

There are two main algorithms to implement this MCM for an efficient FIR filter design: 1) graph based algorithms and 2) common subexpression elimination (CSE) algorithms. Some techniques have been introduced for efficient reconfigurable constant multiplier design [1]-[2], for many applications where the filter coefficients are change in real time. Binary common sub-expression elimination (BCSE) algorithm is one of the techniques for designing an efficient constant multiplier, and used for low complexity reconfigurable FIR filters.

2. MULTIPLE CONSTANT MULTIPLICATION

Multiplication with constant is called as constant multiplication. By multiplying input with multiple numbers of specific coefficients to produce multiple outputs is called MCM [3]. Multiplication can be performed by shifting and adding operations. Constant multiplier consists of adder, subtractor and shifter according to the coefficient pair.

\[
\begin{align*}
X & \quad \text{ADDER AND} \\
& \quad \text{SHIFTERS} \\
Y_1 &= \alpha_1 X \\
Y_2 &= \alpha_2 X
\end{align*}
\]

Fig. 1. MCM operation

X denotes input, \(\alpha_1\) and \(\alpha_2\) are filter coefficients, \(Y_1\) and \(Y_2\) are the outputs in Fig1. MCM technique is very complex that is believed to be NP-hard. Serial data input is multiplied with two pair of coefficients and produces \(Y_1\), \(Y_2\) outputs.

3. COMMON SUBEXPRESSION ELIMINATION

A CSE algorithm is one of the most efficient methods for reducing the number of adders used to realize the multipliers for representing filter coefficients in binary form[10]. The BCSE algorithm deals with the elimination of redundant binary common sub-expression that occurs within the coefficients [11]. In BCSE technique redundant computations can be eliminated from coefficient multipliers by reusing the common binary bit patterns present in the coefficients. In an n-bit binary number, the number of BCSs can be formed as \(2n-(n+1)\). CSE is more efficient than MCM.
4. VERTICAL-HORIZONTAL BCSE ALGORITHM

The BCSE algorithm consists of three techniques binary horizontal subexpression elimination (HBCSE), binary vertical subexpression elimination (VBCSE) and hardwiring of the final stages, which will reduces the number of adders used. VBCSE produces more effective BCS elimination than the HBCSE. The combination of vertical and horizontal BCSE (VHBCSE) algorithm [4] is used for an efficient reconfigurable FIR filter. The procedure of application of the 8-Tap symmetric FIR filter has been depicted graphically in Fig.2.

![Fig. 2. Application procedure for VHBCSE algorithm](image)

Firstly, most common horizontal subexpression resulting from the matrix table in the MCM, and then remaining non-zero bits is examined for optimum vertical common subexpression [5]-[9]. The binary format of the given example is shown in Fig.3. It consumes less area than MCM.

5. PROPOSED SUB-SUBTRACTION ALGORITHM

In VHBCSE algorithm adders are used in filter design. It consumes more area and power. In order to reduce area and power subtractor is used instead of adders in the filter design. The data flow diagram of the proposed sub-subtraction algorithm based on constant multiplier (CM) design is shown in Fig.4.

![Fig. 4. Data flow diagram](image)

The designed multiplier considers the length of the input (Xin) and coefficient (H) as 16-bit and 17-bit respectively when the output is assumed to be 16-bit long. The inputs that are sampled stored first in the register then the coefficients are directly stored in the LUTs.

![Fig. 5. Sign conversion block hardware architecture](image)

A. Sign conversion block

Sign conversion block is used to convert the signed decimal data representation of both the input and the coefficient. The hardware architecture of the signed conversion block is shown in Fig.5. It consist of one 1’s completer circuit used to convert the inverted version of the 16-bit (excluding MSB) of the coefficient. The one 2:1 multiplexer is used to generate the multiplexed coefficients depend on the most significant bit value of the coefficient.

If the value of the original coefficient is negative, the coefficient that is multiplexed will be in the inverted form; otherwise it will remain the same.

![Fig. 6. Block diagram of partial product generator unit](image)

B. Partial product generator (PPG)

The shift and add technique has been used to generate the partial product in the BCSE method. The partial products that are generated are summed up in the following layers to produce the final multiplication result. The block diagram is shown in Fig.6.

C. Multiplexes unit

The multiplexers unit are used to select the data generated from the PPG unit depends on the coefficient’s binary value.
The architecture of the multiplexers unit is shown in Fig. 7. At layer 1, eight 4:1 multiplexers are used to produce the partial products.

D. Controlled subtraction at Layer-2
The partial products that are generated by the eight groups of groups of 2-bit BCSs are added for the final multiplication results that are performed in the three layers.

E. Controlled subtraction at Layer-3
The four multiplexed values generated from the layer-2 are subtracted in the layer-3.

F. Final addition on Layer-4
This block is used to produce the final multiplication result between the input and the coefficient. The block diagram for overall constant multiplication is shown in Fig. 7.

Fig. 7. Proposed reconfigurable constant multiplier architecture

6. HARDWARE IMPLEMENTATION RESULTS AND DISCUSSIONS
The sub-subtraction algorithm based constant multiplier architecture has been coded using VHDL hardware description language to synthesize in the targeted FPGA device using Xilinx ISE 9.2i synthesis tool. Analysis of the existing VHBCSE algorithm in terms of area, power and delay has been presented in Table 1.

<table>
<thead>
<tr>
<th>PARAMETERS</th>
<th>16-BIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>DELAY</td>
<td>56.677ns</td>
</tr>
<tr>
<td>NO. OF SLICES</td>
<td>414</td>
</tr>
<tr>
<td>NO. OF LUTs</td>
<td>786</td>
</tr>
<tr>
<td>NO. OF IOs</td>
<td>33</td>
</tr>
<tr>
<td>NO. OF BONDED IOs</td>
<td>33</td>
</tr>
<tr>
<td>POWER</td>
<td>405mW</td>
</tr>
</tbody>
</table>

TABLE 1 - ANALYSIS OF PROPOSED SUB-SUBTRACTION ALGORITHM

<table>
<thead>
<tr>
<th>PARAMETERS</th>
<th>SUB-SUBTRACTION ALGORITHM [16-BIT]</th>
</tr>
</thead>
<tbody>
<tr>
<td>DELAY</td>
<td>53.416ns</td>
</tr>
<tr>
<td>NO. OF SLICES</td>
<td>318</td>
</tr>
<tr>
<td>NO. OF LUTs</td>
<td>594</td>
</tr>
<tr>
<td>NO. OF IOs</td>
<td>33</td>
</tr>
<tr>
<td>NO. OF BONDED IOs</td>
<td>33</td>
</tr>
<tr>
<td>POWER</td>
<td>380mW</td>
</tr>
</tbody>
</table>

Compared with the existing algorithm the area, power and delay has been reduced in the sub-subtraction algorithm.

7. CONCLUSION
In this paper, an efficient fixed point reconfigurable FIR filters has been implemented using vertical-horizontal BCSE algorithm have been studied. The impacts of power consumption, delay, area have been analyzed. Simulation results have been found for existing method. The use of adders in existing method increases area and power consumption. To overcome these drawbacks, subtractor is used. The subtractor is to be used to improve the power, minimize delay and reduce area instead of adders. Then the technique is to be implemented in Spartan 3E.

REFERENCES


