IMAGE SEGMENTATION BASED ON DILATION AND EROSION TO REDUCE BACKGROUND NOISE

T.Bhuvaneswari\(^1\), K.P.Keerthana\(^2\)

\(^1\)(Dept of ECE, Asst. Professor, KGiSL Institute of Technology, Coimbatore, India, bhuvaneswari3008@gmail.com)
\(^2\)(Dept of ECE, Asst. Prof, KGiSL Institute of Technology, Coimbatore, India, keerthanaete@gmail.com)

Abstract — Mathematical morphology is a powerful tool for image processing and analysis in a wide range of applications, including shape recognition, image processing, and video processing document authentication and computer vision. The basic binary morphological operations are dilation and erosion. Either of the two operations has two operands the input signal, which is usually an image, and the structuring element characterized by its shape, size, and center location. The other binary morphological operations such as opening, closing, hit-and-miss, and operation between the images operation are based on various combinations of the two basic operations, dilation, and erosion. A binary image is segmented into different parts, which are processed with different structuring elements in the basic binary compute units. Then, the processing results are combined to form an entire image. To reduce the background noise and to get clean image we going for this binary morphological operation.

Keywords — Single instruction multiple data, Reconfigurable binary processing module.

1. INTRODUCTION

The main objective of this binary morphological operation using dilation, erosion, opening and closing to reduce the background noise and to get the clean image. In this, there are two inputs, one is an image and another one is structuring element. Structuring element differs for different images. Structuring element is like a mask as in different sizes (3*3), (5*5). The input image is masking with the structuring element, the image pixels are exactly fits with mask then the erosion will be done the image pixels anyone hits with mask then the dilation will be done. Erosion followed by dilation is opening process, dilation followed by erosion is closing process.

2. OVERVIEW

Binary image processing is extremely useful in various areas, such as object recognition, tracking, motion detection and machine intelligence, image analysis and understanding video processing, computer vision and identification and authentication systems. Binary image processing has been commonly implemented using processors such as CPU or DSP. However, it is inefficient and difficult to use such processors for binary image processing. High-speed implementation of binary image processing operations can be efficiently realized by using chips specialized for binary image processing. Therefore, binary image processing chips have attracted much attention in the field of image processing. Application-specific chips and hardware have been reported for various applications. A chip with cellular-logic processing array was implemented to enhance and verify fingerprint images.

All the above mentioned chips are designed for specific applications. The major drawback of application-specific chips is the lack of flexibility. With the continuous CMOS technology scaling, importance of flexibility exceeds that of silicon area, especially in vision chips. The reconfigurable technique can bridge the gap between application-specific integrated circuits and flexibility. A vision system with high flexibility and performance, small size, and low power consumption can be implemented in a single chip. Most reconfigurable vision chips realize reconfigurable computing by processing an element array. They can be used in image or video processing, target tracking, multimedia applications, and computer vision. Reconfigurable binary image processing chips have been designed to generalize the binary image applications of a chip. Chips were presented to perform basic binary morphological operations, such as dilation, erosion, opening, and closing. Programmable analog vision processors based on the cellular neural or nonlinear network universal machine architecture were proposed for a wide range of applications such as motion analysis and texture classification. A programmable single instruction multiple data (SIMD) real-time vision chip was presented to achieve high-speed target tracking. In a programmable binary morphology coprocessor was introduced to the visual content analysis engine of the chip used for visual surveillance. A reconfigurable image processing accelerator incorporating eight macro processing elements was designed to support real-time change detection and background registration based on video object segmentation algorithm. Recently, a vision chip with the architecture of a massively parallel cellular array of processing elements was presented for image processing by using the asynchronous or synchronous processing technique. It has been a common practice to build application-specific chips for real-time binary image processing. However, such chips have a limited application range. On the other hand, the general-purpose binary image processing chips mentioned above have their...
own problems. Some of these chips are made of analog circuit and some are made up of an analog part and a digital part. When compared with the digital part, the analog part shows low robustness, accuracy, and scalability although it has a small area and low power consumption. Other general-purpose chips have the architecture of a digital processor array, in which each digital processor handles one pixel. When large sized images are processed, the chips will become extremely large. To design a high performance, small size, and wide application range chip for real-time binary image processing. A binary image processor that consists of a reconfigurable binary processing module, including re-configurable binary compute units and output control logic, input and output image control units, and peripheral circuits. The reconfigurable binary compute units are of a mixed-grained architecture, which has the characteristics of high flexibility, efficiency, and performance. The performance of the processor is enhanced by using the dynamic reconfiguration approach. The processor is implemented to perform real-time binary image processing. It is found that the processor can process pixel-level images and extract image features, such as boundary and motion images. Basic mathematical morphology operations and complicated algorithms can easily be implemented on it. The processor has the merit of high speed, simple structure, and wide application range. Some of these chips are made of analog circuit and some are made up of an analog part and a digital part. They can be used in image or video processing, target tracking, multimedia applications, and computer vision.

3. ARCHITECTURE OF BINARY IMAGE PROCESSOR

The presented processor is designed for applications in image or video processing, computer vision, machine intelligence, and identification and authentication systems. Such systems should have a high flexibility, efficiency, and high performance processor for wide applications; therefore, the processor design is focused on high flexibility and speed. Some of the conventional works are designed for specific applications and some have large areas and high power consumption. Then, reconfigurable binary processing module with high speed and simple structure is implemented for wide use and consuming fewer hardware resources.

![Diagram of Binary Image Processor](image)

The core of the processor is a reconfigurable binary processing module consisting of binary compute units and output control logic. The processor also has two bus interfaces, the input and output control logic units, the process control unit, and a configuration register group.

4. RECONFIGURABLE BINARY PROCESSING MODULE

The diagram of the reconfigurable binary processing module (RBPM) is given in Fig 2. It can be divided into two main parts. The architecture of the binary compute unit each binary compute unit, which has two binary compute elements and one set of operation elements, can perform logic reduction, median filtering, and set operations. The binary compute unit has a mixed-grained architecture that has high flexibility, efficiency, and performance, and short reconfiguration time. Granularity refers to the level of data manipulation. Usually, two types of granularity are distinguished as fine-grained, which corresponds to the bit-level manipulation of data, and coarse-grained, which corresponds to the word level. The fine-grained architecture is highly flexible, and the coarse-grained architecture has fewer reconfiguration parameters and is highly efficient. The mixed-grained architecture is more flexible and efficient than the coarse-grained architecture.

![Diagram of Reconfigurable Binary Processing Module](image)

The first part is the output control logic, which selects the output from all the binary compute unit outputs according to the given parameters and converts the series data of 1-b binary images into parallel data. The second part consists of several binary compute units that perform binary logic and binary image operations at a high speed. The binary image algorithms are realized by the operations in the individual binary compute units and the connection pattern of these units. The units can execute binary image operations in a pipelined. The operation executed in a binary compute unit is decided by configurable registers, including operation parameters, image resolution parameters; mask sizes, input and output selection parameters, and auxiliary parameters. The set operation element can perform binary set operations, such as union, intersection, complement, subtraction, addition, and straight through output. The inputs of the set operation element and the outputs of the binary compute unit are trans-mitted via two sets of multiplexers, respectively, which makes the unit architecture more flexible.
5. BINARY MATHEMATICAL MORPHOLOGY

The basic binary morphological operations are dilation and erosion. Either of the two operations have two operands the input signal, which is usually an image, and the structuring element characterized by its shape, size, and center location. The other binary morphological operations such as opening, closing, and hit-and-miss operation are based on various combinations of the two basic operations, dilation, and erosion. MM is most commonly applied to digital images, but it can be employed as well on graphs, surface meshes, solids, and many other spatial structures.

A. EROSION OPERATION

We are giving two inputs, one is an image and another one is structuring element. Structuring element its differs for different images. Structuring element is like a mask as in different sizes (3*3), (5*5).

![Fig 3: Block Diagram of Erosion](image)

We are masking the input image with the structuring element, the image pixels are exactly fits with an mask replace the origin with '1' or else '0'. we moving the mask over an image in each row wise and column wise. Finally we get an erosion output. Erosion can split apart joined objects.

![Fig 4: Erosion Example 1](image)

Erosion can strip away extrusions

![Fig 5: Erosion Example 2](image)

The basic effect of the operator on a binary image is to erode away the boundaries of regions of foreground pixels. Thus areas of foreground pixels shrink in size, and holes within those areas become large.

Strip away a layer of pixels from an object, shrinking it in the process. If for every pixel in the structuring element, the corresponding pixel in the image underneath is a foreground pixel, then the input pixel is left as it is. If any of the corresponding pixels in the image are background, however, the input pixel is also set to background value. Erosion shrinks objects.

![Fig 6: Effect of erosion using a 3×3 square structuring element](image)

B. DILATION OPERATION

We are giving two inputs, one is an image and another one is structuring element. Structuring element its differs for different images. Structuring element is like a mask as in different sizes (3*3), (5*5).

![Fig 7: Block Diagram of Dilation](image)

We are masking the input image with the structuring element, the image pixels anyone hits with an mask replace the origin with '1' or else '0'. Thus we have getting a dilation output. Dilation enlarges objects. The dilation operator takes two pieces of data as inputs. The first is the image which is to be dilated. The second is a (usually small) set of coordinate points known as a structuring element (also known as a kernel). It is this structuring element that determines the precise effect of the dilation on the input image.

![Fig 8: Dilation Example 1](image)

Dilation can repair breaks

![Fig 9: Dilation Example 2](image)

The basic effect of the operator on a binary image is to gradually enlarge the boundaries of regions of foreground pixels (i.e. white pixels, typically). Thus areas of foreground...
pixels grow in size while holes within those regions become smaller. If at least one pixel in the structuring element coincides with a foreground pixel in the image underneath, then the input pixel is set to the foreground value. If all the corresponding pixels in the image are background, however, the input pixel is left at the background value. The dilation operator takes two pieces of data as inputs. The first is the image which is to be dilated. The second is a set of coordinate points known as a structuring element, dilation can repair breaks and also dilation can repair intrusions.

**Fig 10:** Effect of dilation using a 3×3 square structuring element

**C. OPENING OPERATION**

More interesting morphological operations can be performed by performing combinations of erosions and dilations. Erosion followed by dilation is opening process. Opening like erosion while erosion eliminates small clumps. The basic effect of an opening is somewhat like erosion in that it tends to remove some of the foreground pixels from the edges of regions of foreground pixels. However it is less destructive than erosion in general. As with other morphological operators, the exact operation is determined by a structuring element. The effect of the operator is to preserve foreground regions that have a similar shape to this structuring element, or that can completely contain the structuring element, while eliminating all other regions of foreground pixels. Very simply, an opening is defined as an erosion followed by a dilation using the same structuring element for both operations. The opening operator therefore requires two inputs: an image to be opened, and a structuring element. The opening of image \( f \) by structuring element \( s \), denoted \( f \circ s \) is simply erosion followed by dilation \( f \circ s = (f - s) + s \)

**Fig 11:** Block Diagram of Opening

**D. CLOSING OPERATION**

More interesting morphological operations can be performed by performing combinations of erosions and dilations. Dilation followed by erosion is closing process. Closing like dilation while dilation enlarges the boundaries. Dilation followed by erosion same structuring element both operations. Expanding Change a pixel from 0 to 1 if any neighbors of the pixel are 1. Shrinking Change a pixel from 1 to 0 if any neighbors of the pixel are 0. Shrinking expanding background expanding followed shrinking used filling undesirable holes. Shrinking followed expanding used removing isolated noise pixels. Expanding and shrinking used to determine isolated components and clusters. Closing is similar in some ways to dilation in that it tends to enlarge the boundaries of foreground (bright) regions in an image (and shrink background color holes in such regions), but it is less destructive of the original boundary shape. As with other morphological operators, the exact operation is determined by a structuring element. The effect of the operator is to preserve background regions that have a similar shape to this structuring element, while eliminating all other regions of background pixels.

**Fig 12:** Effect of opening using a 3×3 square structuring element

**Fig 13:** Block Diagram of Closing

Closing is opening performed in reverse. It is defined simply as dilation followed by an erosion using the same structuring element for both operations. The closing operator therefore requires two inputs an image to be closed and a structuring element. The closing of image \( f \) by structuring element \( s \), denoted \( f \cdot s \) is simply a dilation followed by an erosion \( f \cdot s = (f + s) - s \) One of the uses of dilation is to fill in small background color holes in images, e.g. 'pepper noise'. One of the problems with doing this, however, is that the dilation will also distort all regions of
pixels indiscriminately. By performing erosion on the image after the dilation, i.e. a closing, we reduce some of this effect. The effect of closing can be quite easily visualized. Closing followed by erosion same structuring element both operations. As with other morphological operators, the exact operation is determined by a structuring element.

Fig 14: Effect of closing using a 3×3 square structuring element

6. RESULT ANALYSIS

The binary image processing system is applied to verify the proposed binary image processor. The system performance is shown in Table I. They selected as the system CPU, and AHB and APB as the system buses. The operations and algorithms are applied on the system. The size of the structuring element is 5 × 5 and the image resolution is 1024 × 1024. Table I shows that the execution time of each operation is less than 5 ms. The frame rate is more than 200 f/s, far exceeding the real-time requirement.

Table I. Comparison of Image Processors

<table>
<thead>
<tr>
<th>Processor</th>
<th>SIMD</th>
<th>Cellular Processor</th>
<th>Reconfigurable morphological image processing accelerator</th>
<th>This Paper</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process</td>
<td>0.18</td>
<td>0.35</td>
<td>0.25</td>
<td>0.18</td>
</tr>
<tr>
<td>Area</td>
<td>0.45</td>
<td>9</td>
<td>27.32</td>
<td>2.56</td>
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<tr>
<td>Memory (bit)</td>
<td>1K</td>
<td>418K</td>
<td>381K</td>
<td>40K</td>
</tr>
<tr>
<td>Image Processing</td>
<td>Binary</td>
<td>Binary &amp; Gray</td>
<td>Binary &amp; Gray</td>
<td>Binary</td>
</tr>
<tr>
<td>Voltage</td>
<td>1.8V</td>
<td>2.5V</td>
<td>2.5V</td>
<td>1.8V</td>
</tr>
<tr>
<td>Power Conumption (mW)</td>
<td>8.72</td>
<td>26.35</td>
<td>600</td>
<td>98.5</td>
</tr>
</tbody>
</table>

The overall performance of the binary image processor is evaluated according to the number of the binary compute units. At a 220-MHz system clock each binary compute unit in the processor can provide 15.18 GOPS in SMIC 0.18-µm CMOS process. The whole reconfigurable binary processing module containing four binary compute units can provide 60.72 GOPS and achieve 23.72 GOPS/mm² area efficiency. The proposed processor is compared with the processor, to be fair, the area and power consumption of the chips are normalized to 0.18-µm CMOS technology. The technology scaling of area and power area

\[ \text{PowerL2} = \text{PowerL1} \times (L2/L1)^2 \times (V/L2/VL1)^2 \]

\[ \text{AreaL2} = \text{AreaL1} \times (L2/L1)^2 \]

Where L1 and L2 are the characteristic lengths of the two different processes.

The basic operations supported by the processors are shown in Table I. The processors support dilation, erosion, opening, and closing, but not hit-and-miss and operations between images. This feature limits the usage of these processors although they are efficient enough for specific applications.

MATLAB RESULT:

File compression output

In the file compression using run length encoding we compress the file size from 284 KB to 4 KB. The input file size is 284 KB and after we doing the process by using run length encoding we get the output file size as 4 KB.

input_butterfly.txt  runlength_out.txt

7. SIMULATION RESULT:

EROSION OUTPUT:
CONCLUSION

By using Morphological binary image processing we can get the noiseless image with the help of basic mathematical morphology operations such as dilation, erosion, opening, closing and algorithms. It can easily be implemented on the processor because of its simple structure. The processor, featured by high speed, simple structure, and wide application range, is suitable for binary image processing, such as object recognition, object tracking and motion detection, computer vision, identification, and authentication. The synthesis results demonstrated that each binary compute unit in the processor can provide 15.18 GOPS and that the binary image processor can deliver 60.72 GOPS and achieve 23.72-GOPS/mm² area efficiency at a 220-MHz system clock in the SMIC 0.18-μm CMOS process. In this we add file compression using run length encoding concept, by using this memory space will be reduced and also adding another concept as operation between images. Operations between the images is that we using OR and AND operation. OR operation performs union AND operation performs intersect. By using this we can find out common part of the images. Suppose if the images merged means we can split the images.

REFERENCES


