Abstract—Video processing systems such as HEVC requiring low energy consumption needed for the multimedia market has lead to extensive development in fast algorithms for the efficient approximation of 2-D DCT transforms. The DCT is employed in a multitude of compression standards due to its remarkable energy compaction properties. Multiplier-free approximate DCT transforms have been proposed that offer superior compression performance at very low circuit complexity. Such approximations can be realized in digital VLSI hardware using additions and subtractions only, leading to significant reductions in chip area and power consumption compared to conventional DCTs and integer transforms. In this paper, we introduce a novel 8-point DCT approximation that requires only 14 addition operations and no multiplications. The proposed transform possesses low computational complexity and is compared to state-of-the-art DCT approximations in terms of both algorithm complexity and peak signal-to-noise ratio. The proposed DCT approximation is a candidate for reconfigurable video standards such as HEVC. The proposed transform and several other DCT approximations are mapped to systolic-array digital architectures and physically realized as digital prototype circuits using FPGA technology and mapped to 45 nm CMOS technology.

1. INTRODUCTION
Recent years have experienced a significant demand for high dynamic range systems that operate at high resolutions. In particular, high-quality digital video in multimedia devices and video-over-Internet protocol networks are prominent areas where such requirements are evident. Other noticeable fields are geospatial remote sensing, traffic cameras, automatic surveillance, homeland security, automotive industry and multimedia wireless sensor networks, to name but a few. Often hardware capable of significant throughput is necessary; as well as allowable area-time complexity. In this context, the discrete cosine transform (DCT) is an essential mathematical tool in both image and video coding. Indeed, the DCT was demonstrated to provide good energy compaction for natural images, which can be described by first-order Markov signals. Moreover, in many situations, the DCT is a very close substitute for the Karhunen-Loève transform (KLT), which has optimal properties. As a result, the two-dimensional (2-D) version of the 8-point DCT was adopted in several imaging standards such as JPEG, MPEG-1, MPEG-2, H.261, H.263, and H.264/AVC. Additionally, new compression schemes such as the High Efficiency Video Coding (HEVC) employs DCT-like integer transforms operating at various block sizes ranging from 4 × 4 to 32 × 32 pixels. The distinctive characteristic of HEVC is its capability of achieving high compression performance at approximately half the bit rate required by H.264/AVC with same image quality.

2. BACKGROUND AND MOTIVATION
In existing radix algorithms generally have a regular computational structure, which reduces implementation complexity. However, due to their recursive nature, radix algorithms are difficult to realize pipeline and are not suitable for high-speed applications. Compared to non radix algorithms, radix algorithms allow us to generate higher-order DCTs from lower-order DCTs.
4. DCT FOR IMAGE AND VIDEO COMPRESSION REQUIRING ONLY 14 ADDITIONS

![Image](Fig1) Approximate transform by 1D approximate transform

The 1-D approximate DCT blocks (Fig. 3.1) implement a particular fast algorithm chosen from the collection described earlier in the paper. The first instantiation of the DCT block furnishes a row-wise transform computation of the input image.

5. APPROXIMATE DCT

Computational complexity An orthogonal approximation for the 8-point discrete cosine transform (DCT) is introduced. The proposed transformation matrix contains only zeros and ones; multiplications and bit-shift operations are absent. Close spectral behavior relative to the DCT was adopted as design criterion. The proposed algorithm is superior to the signed discrete cosine transform. It could also outperform state-of-the-art algorithms in low and high image compression scenarios, exhibiting at the same time a comparable.

6. IMAGE PROCESSING

A. COMPRESSION

Image compression is an important topic in the digital world. Whether it be commercial photography, industrial imagery, or video. A digital image bitmap can contain considerably large amounts of data causing exceptional overhead in both computational complexity as well as data processing. Storage media has exceptional capacity; however, access speeds are typically inversely proportional to capacity. Compression is important to manage large amounts of data for network, internet or storage media. Compression techniques have been studied for years, and will continue to improve. Typically image and video compressors and decompressors (CODECS) are performed mainly in software as signal processors can manage these operations without incurring too much overhead in computation. However, the complexity of these operations can be efficiently implemented in hardware. Hardware specific CODECS can be integrated into digital systems fairly easily. Improvements in speed occur primarily because the hardware is tailored to the compression algorithm rather than to handle a broad range of operations like a digital signal processor. Data compression itself is the process of reducing the amount of information into a smaller data set that can be used to represent, and reproduce the information. Types of image compression include lossless compression, and lossy compression techniques that are used to meet the needs of specific applications.

JPEG compression can be used as a lossless or a lossy process depending on the requirements of the application. Both lossless and lossy compression techniques employ reduction of redundant data. Work in standardization has been controlled by the International Organization for Standardization (ISO) in cooperation with the International Electro technical Commission (IEC). The Joint Photographic Experts Group produced the well-known image format JPEG, a widely used image format. JPEG provides a solid baseline compression algorithm that can be modified numerous ways to any desired application. The JPEG specification was released initially in 1991, although it does not specify a particular implementation.

B. DECOMPRESSION

The compression phase is reversed in the decompression process, and in the opposite order. The first step is restoring the Huffman tables from the image and decompressing the Huffman tokens in the image. Next, the DCT values for each block will be the first things needed to decompress a block. The other 63 values in each block are decompressed by JPEG, filling in the appropriate number of zeros. The last step is combined of decoding the zigzag order and recreating the 8 x 8 blocks .The inverse DCT(IDCT) takes each value in the spatial domain and examines the contributions that each of the 64 frequency values make to that pixel.

C. DISCRETE COSINTRANSFORM

A discrete cosine transform (DCT) expresses a finite sequence of data points in terms of a sum of cosine functions oscillating at different frequencies. DCTs are important to numerous applications in science and engineering, from lossy compression of audio (e.g. MP3) and images (e.g. JPEG) (where small high-frequency components can be discarded), to spectral methods for the numerical solution of partial differential equations. The use of cosine rather than sine functions is critical for compression, since it turns out (as described below) that fewer cosine functions are needed to approximate a typical signal, where as for differential equations the cosines express a particular choice of boundary conditions.
In particular, a DCT is a Fourier-related transform similar to the discrete Fourier transform (DFT), but using only real numbers. DCTs are equivalent to DFTs of roughly twice the length, operating on real data with even symmetry (since the Fourier transform of a real and even function is real and even), where in some variants the input and/or output data are shifted by half a sample. There are eight standard DCT variants, of which four are common. The most common variant of discrete cosine transform is the type-II DCT, which is often called simply "the DCT" and its inverse, the type-III DCT, is correspondingly often called simply "the inverse DCT" or "the IDCT". Two related transforms are the discrete sine transform (DST), which is equivalent to a DFT of real and odd functions, and the modified discrete cosines transform (MDCT), which is based on a DCT of overlapping data.

D. ADDERS

Addition usually impacts widely the overall performance of digital systems and a crucial arithmetic function. In electronic applications adders are most widely used. Applications where these are used are multipliers, DSP to execute various algorithms like FFT, FIR and IIR. Wherever concept of multiplication comes adders come in to the picture. As we know millions of instructions per second are performed in microprocessors. So, speed of operation is the most important constraint to be considered while designing multipliers. Due to device portability miniaturization of device should be high and power consumption should be low. Devices like Mobile, Laptops etc. require more battery backup. So, a VLSI designer has to optimize these three parameters in a design. These constraints are very difficult to achieve so depending on demand or application some compromise between constraints has to be made.

\[ S_i = A_i \oplus B_i \oplus C_i \]

\[ C_{i+1} = A_i B_i + (A_i + B_i) C_i \] where \( i = 0, 1, ..., n-1 \)

Ripple carry adders exhibits the most compact design but the slowest in speed. Whereas carry look ahead is the fastest one but consumes more area. Carry select adders act as a compromise between the two adders. In 2002, a new concept of hybrid adders is presented to speed up addition process by Wang et al. that gives hybrid carry look-ahead/carry select adders design. In 2008, low power multipliers based on new hybrid full adders is presented in . In 2008, HasanKrad et al provided the performance analysis for a 32-Bit Multiplier with a Carry look ahead Adder and a 32-bit Multiplier with a Ripple Adder using VHDL and showed that CLA multiplier is almost double in speed as compared to RCA multiplier.

7. SIMULATION RESULT

ModelSim is a hardware simulation and debug environment primarily targeted at smaller ASIC and FPGA design. ModelSim combines simulation performance and capacity with the code coverage and debugging capabilities required to simulate multiple blocks and systems and attain ASIC gate-level sign-off. Comprehensive support of Verilog, SystemVerilog for Design, VHDL, and SystemC provide a solid foundation for single and multi-language design verification environments. ModelSim’s easy to use and unified debug and simulation environment provide today’s FPGA designers both the advanced capabilities that they are growing to need and the environment that makes their work productive. ModelSim is a verification and simulation tool for VHDL, Verilog, SystemVerilog, and mixed language designs.

8. COMPRESSION

MODEL SIM

![Fig 3) Modelsim Output(Compression)](image)
In this paper, we proposed (i) a novel low-power 8-point DCT approximation that require only 14 addition operations to computations and (ii) hardware implementation for the proposed transform and several other prominent approximate DCT methods, including the designs by Bouguezel-Ahmad-Swamy. We obtained that all considered approximate transforms perform very close to the ideal DCT. However, the modified CB-2011 approximation and the proposed transform possess lower computational complexity and are faster than all other approximations under consideration. In terms of image compression, the proposed transform could outperform the modified CB-2011 algorithm. Hence the new proposed transform is the best approximation for the DCT in terms of computational complexity and speed among the approximate transform examined. Introduced implementations address both 1-D and 2-D approximate DCT. All the approximations were digitally implemented using Xilinx tools. Therefore, the proposed architectures are suitable for image and video processing, being candidates for improvements in several standards including the HEVC. Future work includes replacing the Free PDK standard cells with highly optimized proprietary digital libraries from TSMC PDK and continuing the CMOS realization all the way up to chip fabrication and post-fab test on a measurement system.

REFERENCES


