# DESIGN OF DESENSITIZED FIR HALFBAND FILTERS FOR MULTIRATE SYSTEMS

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***Abstract—*** *The desensitized FIR filter using Vedic multiplier is presented to achieve higher operating speed. Vedic mathematics utilizes less computation time. The performance of proposed desensitized filter using Vedic multiplier is compared with conventional filter using array multiplier. The evaluation carried out through simulation and functional verification in order to highlight the speed superiority by reducing the computation time. The simulation and analysis is done by using Modelsim 10.1b and synthesized using Xilinx ISE 9.2i.*

***Keywords— Desensitized FIR filter; Vedic multiplier; Array multiplier; Multirate systems***

## 1. INTRODUCTION

Among several digital filters are a type of most important filter. The conventional digital filters are widely used as versatile building blocks in the application of multirate system. Multirate system means that the system with multiple sampling rates. filters are used in up Sampling and down sampling converters when the sampling rate change is required. However the design of FIR filter has the drawback of higher co-efficient sensitivity and lower operating speed. The further desensitized FIR filters are employed to reduce the sensitivity of the filter to co-efficient by further cascading of block (1+z-1) [1]. In the existing digital half band filters one new method is used for the design and implementation of low power FIR half band filters. In that the frequency response provided with the significant insensitivity to the filter tab coefficient values [2]. In the optimal factoring of FIR filters the filter is designed by using scaled sequence of stages. Each stage has its transfer function factor [3].But it increases the delay of the filter. The existing further desensitized FIR filter uses the conventional array multiplier which requires higher operating speed it also reduce the speed of the filter. In the proposed method Vedic multiplier is used instead of conventional Array multiplier in order to achieve higher speed.

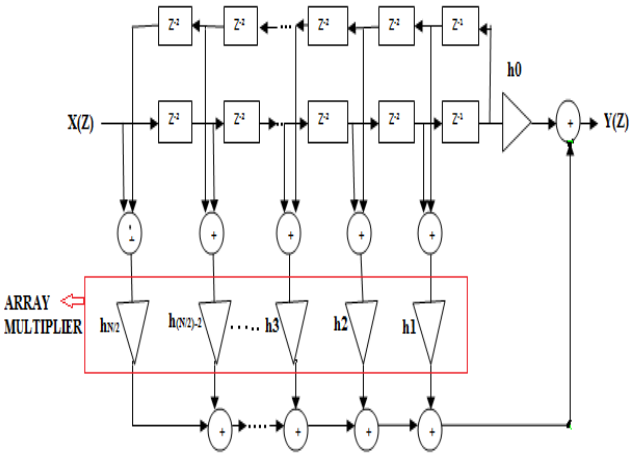


Fig.1. FIR halfband Nth-order filter 1. Direct form

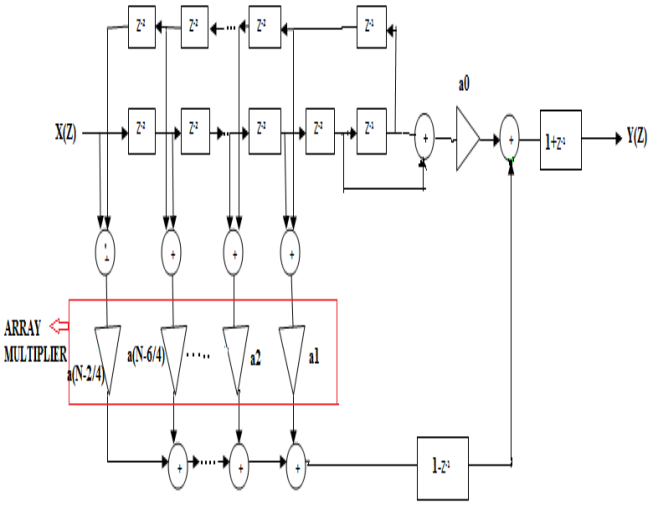


Fig. 2. Desensitized Nth-order FIR half band filter.

Section 2 illustrates the design of desensitized block and section 3 shows the filter design using Vedic multiplier. Section 4 shows the result analysis.

## 2. DESIGN OF DESENSITIZED BLOCK

Figure 1 shows the conventional direct form realization of N-th order FIR half band filter, in which N indicates an even integer such that it uses N register, N/2 +1 adders and (N+2)/2 co-efficient. The coefficients are (h0,h1,h3,h5,h7..hN/2). Based on the basic property of the half band filter the even number coefficients become zero and the coefficient h0 always has the value of 1/2.

The desensitized FIR half band filter can be designed by the addition of block (1+z-1) in the conventional filter structure such design is shown in figure 2. The transfer function of this block has its zero at z=-1. It is also written as $z=e^{j\omega}$ that means $|H(e^{j\omega})|=0$ at $\omega=\pi$. For any type of half band filter the magnitude of the transfer function should satisfy $|H(e^{j\omega})|=0$ at $\omega=\pi$. There are two paths are available from the input to output which may differ in number of coefficients include.

The relationship between the two coefficients $a_k$ and $h_k$ are:

For filter having length=3

$h_0=2a_0 \quad h_1=a_0$

For length=7

$h_0=2a_0 \quad h_1=a_0-a_1 \quad h3=a_1$

For length=11

$h_0=2a_0 \quad h_1=a_0-a_1 \quad h_3=a_1-a_2 \quad h_5=a_2$

The relationship between the coefficients is expressed also in terms of matrix.

## 3. Design Of Desensitized Fir Filters Using Vedic Multiplier

In digital signal processing high speed multiplication plays an important role. Desensitized FIR filter with high speed is achieved with the use of Vedic multiplier. The main advantage of using this Vedic Multiplier is it can be used for multiplication of all the type of numbers and also it requires less computation time compared to other multipliers.

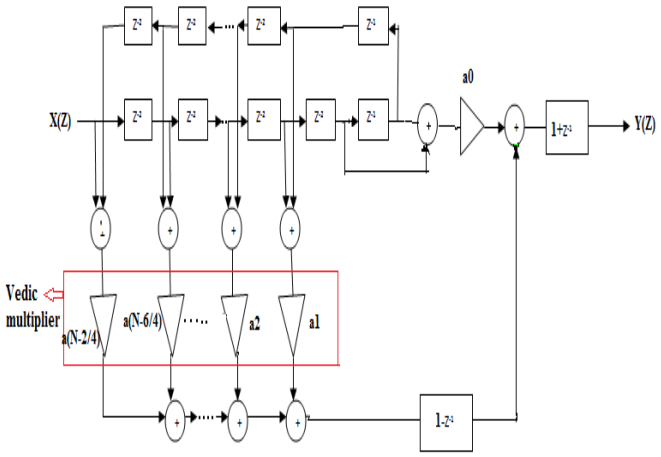


Fig.3.Desensitized FIR half band filter using Vedic multiplier.

## 4. Result Analysis

The results are obtained for conventional direct form FIR filter using array multiplier, desensitized half band FIR filter using array multiplier, and the proposed desensitized FIR half band filter using Vedic multiplier. The coding are developed by using VHDL language and are simulated on Modelsim software. Those are also implemented on FPGA.

The conventional array multiplier can be used in most of the all type of filter design. Fig.4 shows the waveform of the conventional array multiplier. It uses the normal multiplication technique in that the least significant bit is multiplied by the multiplier after that the next bit to the least significant is multiplied by the multiplier and it will be added with the previous result after shifting one bit. This process will be repeated until it reaches the most significant of the multiplicand. The main drawback of this multiplier is its delay and area utilization. For larger number of bits it probably increase the delay when using thin on the filter design it further decrease the speed of the filter.


Fig.4.Waveform of conventional array multiplier

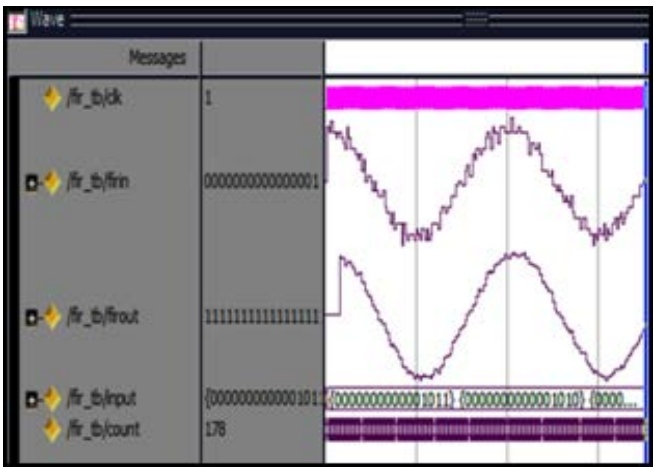


Fig.5.Waveform of direct form FIR filter using array multiplier

The direct form realization of normal FIR filter using array multiplier is shown in Fig.5. In that the noise present on the input wave will be eliminated by using this low pass FIR filter. That is the sudden variations while changing input will be removed.

The main drawback is that it increases the coefficient sensitivity of the filter. In order to reduce the hardware coefficient sensitivity the desensitized FIR half band filters are used. The fig.6.shows the wave form of desensitized FIR half band filters using array multiplier.

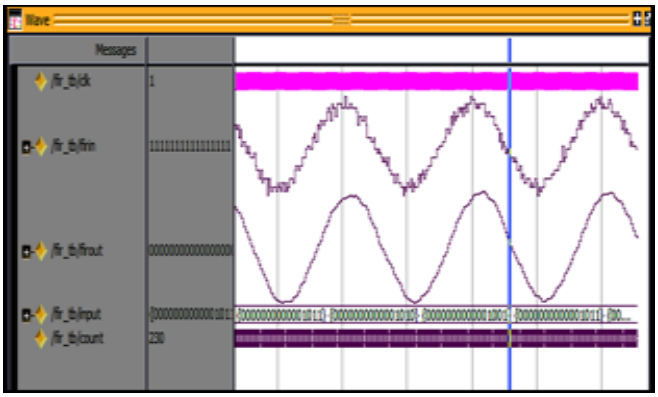


Fig.6.Waveform of desensitized FIR half band filter using array multiplier

The array multiplier in the desensitized FIR half band filter can be replaced by the Vedic multiplier. The Fig.7.shows the wave form of 16x16 Vedic multiplier.

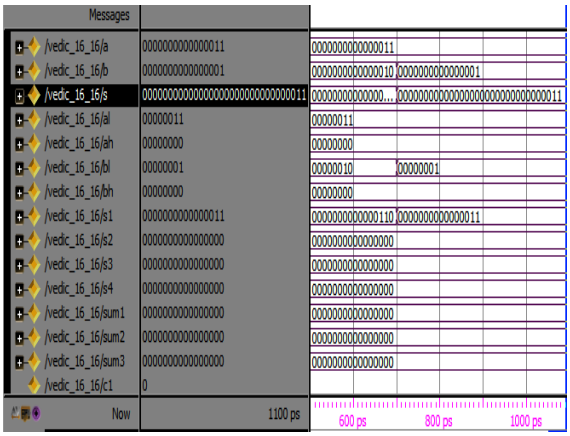


Fig.7.Wave form of the 16 bit Vedic multiplier

The Vedic multiplier architecture follows the vertical and crosswise multiplication algorithm of ancient Indian Vedic mathematics. The two 4-bit numbers multiplicand and multiplier are split into two 2-bit numbers. Thus four 2x2 multiplier are required for 4-bit multiplication. Consider the two 4-bit numbers are M0,M1,M2,M3 and S0,S1,S2,S3.

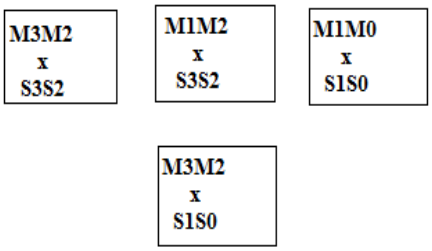


Fig.8.Vedic multiplier structure for 4x4 bit

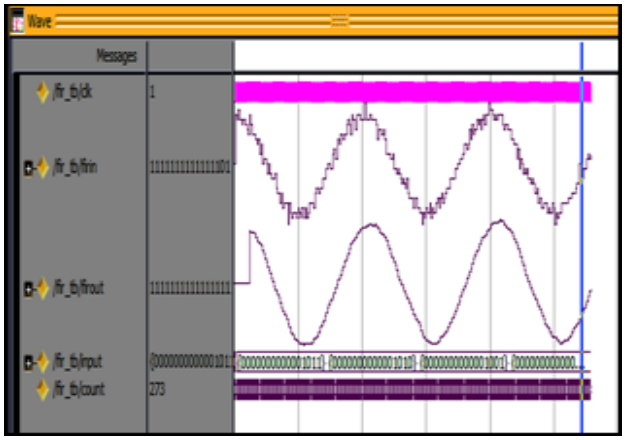


Fig.9. Waveform of desensitized FIR halfband filter using Vedic multiplier

Each block can be processed by using AND gate and addition carried by half adder. The 16 x 16 bit Vedic multiplier is used in the filter design to achieve higher operating speed. Fig.9.shows the wave form of the desensitized FIR half band filters using Vedic multiplier. The proposed filter uses the ripple carry adder for addition and D flip flop for delay block. The sensitivity of the coefficients to the filter can be reduced by the use block (1+z-1). Half band filter requires less number of multiplier block compared to the other filter structure since the even number coefficients are always zero.

## 5. Filter Synthesis Report

The table-1 shows the comparison of delay, number of slices, number of LUT's and power of the conventional FIR filter, desensitized FIR filter using array multiplier and Vedic multiplier.

TABLE 1: Comparison of values

| | Delay | Num. Of LUT's | Num. Of slices | Power( mW) |
|---|---|---|---|---|
| Conventional filter using array multiplier | 53.5ns | 1013 | 224 | 456 |
| Desensitized FIR filter using array multiplier | 55.7ns | 1640 | 225 | 501 |
| Desensitized FIR filter using Vedic multiplier | 53.4ns | 1313 | 209 | 483 |

## 6. Conclusion

Thus the desensitized FIR half band filter was designed by using Vedic multiplier. The delay and device utilization values are compared. Hence the proposed desensitized filter consumes less power and drastically reduces the delay of the system. Future development of this paper is the sensitivity of the filter can be further reduced by adding the block (1+z-1)2.

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