NOVEL LOW POWER HALF-SUBTRACTOR USING AVL WITH SLEEP TRANSISTOR TECHNIQUE BASED ON 0.18µM CMOS TECHNOLOGY

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Abstract— *Now a day's arithmetic circuit plays an important role in designing of any VLSI sys-tem. Subtractor is one of them , in this paper half-subtractor is designed by using the adaptive voltage with sleep transistor technique. This design consumes less power as compare to AVLG and AVLS technique. The AVL with Sleep transistor technique shows the significant reduction in power consumption and propagation delay. This design is much useful in designing the system that consumed less power. The circuit is simulated on cadence tool in 180nm CMOS technology.*

Keywords— AVL Technique; VLSI; Low Power; Half-Subtractor; Sleep Transistor

1. INTRODUCTION

The simplest combinational circuit which performs the arithmetic subtraction of two binary digits is called half-Subtractor. The half-subtractor is a combi-national circuit which is used to perform subtraction of two bits. It has two inputs, X (minuend) and Y (subtrahend) and two outputs D (difference) and B (borrow). The logic symbol and logic diagram, truth table are shown below.

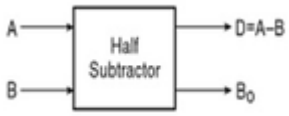

Figure 1: logic symbol of half-subtractor

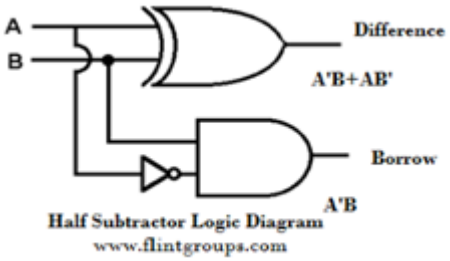

Figure 2: logicdiagram of half subtractor

TABLE 1:TRUTH TABLE OF HALF SUB-TRACTOR

Half Subtractor-Truth Table			
Input		Output	
A	B	Difference	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Figure 1.2 shows the logic diagram ofhalf-subtractor from table 1.1logic expression for Difference output and Borrow output can be written as

$$D = A \oplus B$$

$$Bout = \bar{A}\,B$$

2. LITERATURE SURVEY

Leakage reduction technique as high leakage currents in deep submicron regimes are becoming a major contributor to total power dissipation of CMOS circuits [1]. An adaptive voltage level(AVL) technique can be used to control circuits and it can be used to reduce the heating, the power consumption has to be reduced and this can be achieved by either of the two schemes. One is AVLS (Adaptive Voltage Level at Supply) in which the supply voltage is reduced and the other one is AVLG (Adaptive Voltage Level at Ground) in which the ground potential is increased Leakage current also place a vital role in designing of any system [2,3].High leakage currents in deep submicron regimes are becoming a major contributor to total power dissipation of CMOS circuits as the threshold voltage, channel length and gate oxide thickness are scaled. This provides the motivation to explore the design of low leakage SRAM cells. A very small leakage current is flowing in designing using AVLS technique [4].The power consumption of the electronic devices can be reduced by adopting different design styles. Adiabatic logic style is said to be an attractive solution for such low power electronic applications.

Also power dissipation is very less here [5]. In Deep-Sub-Micron (DSM) technology, it is coming as challenges, e.g., leakage power, performance, data retention, and stability issues. In this work, we have pro-posed a novel low-stress SRAM cell, called as IP3 SRAM bit-cell, as an integrated cell. It has a separate write sub-cell and read sub-cell, where the write sub-cell has dual role of data write and data hold.

The data read sub-cell is proposed as a PMOS gated ground scheme to further reduce the read power by lowering the gate and sub-threshold leakage currents. The drowsy voltage is applied to the cell when the memory is in the standby mode [6]. Scaling of supply voltage and technology for microprocessors to achieve low-power and high-performance. Functionality of special circuits in the presence of high leakage, SRAM cell stability, bit line delay scaling, and power consumption in clocks & interconnects, will be the primary design challenges in the future. Soft error rate control and power delivery pose additional challenges [7].

3. PROPOSED SYSTEM

Arithmetic circuits play a vital role in designing of any VLSI system. Subtractor is one of them. In this paper, Half-Subtractor is being designed using Adaptive Voltage Level (AVL) techniques. This design consumed less power as compare to conventional design. We can reduce the value of total power dissipation by applying the AVLG (adaptive voltage level at ground) technology in which the ground potential is raised and AVLS (adaptive voltage level at supply) in which supply potential is increased. The design is much useful in designing the system that consumed less power.

In conventional Half- Subtractor, a simple transistor level circuit is designed. Where, all NMOS are connected to ground terminal and all P-MOS are connected to Source terminal. The circuit is designed using CMOS and whole circuit consists of 6 transistors. In which 3 NMOS transistors and 3 P-MOS transistors are employed. Leakages current also place a vital role in designing of any system. It should be as low as possible. Power consumption is also an important parameter in system design.

An adaptive voltage level technique can be used to control circuits and it can be used either at the upper end of the cell to bring down the supply voltage value , called AVLS scheme or at the lower end of the cell to lift the potential of the ground node , called AVLG scheme. By this technique reduction of power dissipation is occurred. The power dissipation is reduced less than conventional design cell.

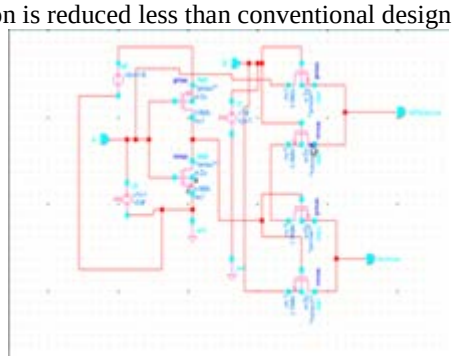

Figure 3: Circuit of conventional half-subtractor

In AVLG technique a combination of 1-N-MOS & 2-P-MOS are connected in parallel. So that a input clock pulse is applied at the NMOS of circuit of AVLG and rest of all P-MOS are connected to ground. This AVLG circuit is connected at the ground terminal of conventional one by removing ground. This ground terminal is connected to the AVLG circuit.

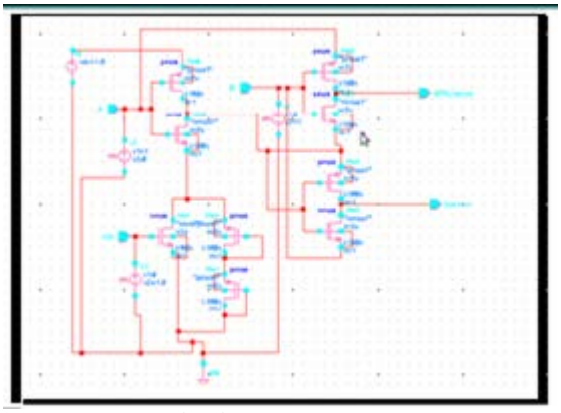

Figure 4:Circuit of half-subtractor incorporated with AVLG

In AVLS technique, a combination of 2- N-MOS & 1-P-MOS are connected in parallel. So that a input clock pulse is applied at the P-MOS of circuit of AVLS and rest of all N-MOS are connected to drain terminal. This AVLS circuit is connected at the voltage supply source terminal of conventional one by removing volt-age supply source. A very small leakage
current is flowing in designing using AVLS technique. Also power dissipation is very less here. By this technique reduction of power dissipation is occurred.

Figure 5: Circuit of half-subtractor incorporated with AVLS

4. ENHANCED SYSTEM

Power consumption and propagation delay is reduced in AVL technique, now a newer technique AVL with sleep transistor can be used to reduce the power consumption and delay. Sleep transistor is either Pmos or Nmos high voltage thresh-old and it can used as a switch to shut off supplies to parts of a design in standby mode. power dissipation can be reduced by involving many techniques. The best method that in practice to reduce leakage power is power gated CMOS circuit. There are two main classifications of power gat-ing , they are Coarse grain power gating and fine grain power gating . In coarse grain power gating, a single sleep transistor is being shared by a large number of circuits. Here the area and power consumed by the sleep transistors are small. However if one of the circuits within this coarse grain domain is active, all the circuits which share the same sleep transistor cannot be set to sleep mode.

In fine grain power gating, each circuit has an individual sleep transistor and hence if any one of the circuit is inactive, the same circuit can be set to sleep mode immediately. Hence the number of sleep transistors in fine grain power gating is much higher than that of coarse grain power gating.

The design of half subtractor us-ing AVLG technique have high power consumption and high delay compared to AVLS ,so we conclude that AVLS is the proper and well suited circuit to control power delay .The below circuit diagram indicates the half subtractor of AVLG technique.

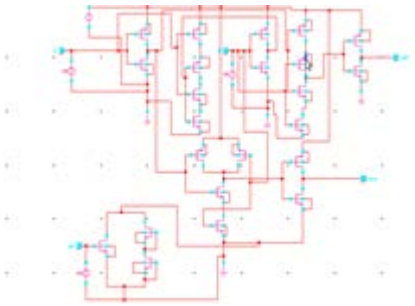

Figure 6: circuit diagram of half sub-tractor AVLG technique

After comparing the half subtrac-tor using AVLS technique provides the efficient output (power & delay),the circuit diagram of half subtractor using AVLS and output wave form can be viewed below

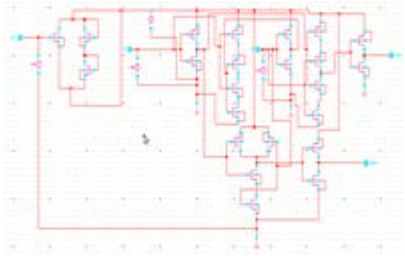

Figure 7:circuit diagram of half subtractor using AVLS technique

The power consumption of power gating circuitry is mainly consumed by the sleep transistor. By applying an AVL with sleep transistor can have resultant power consumption and delay compared to AVLS technique ,the below diagram shows the half subtractor AVL with sleep transistor

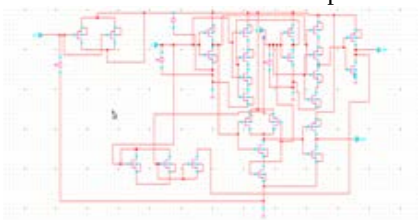

Figure8: Circuit diagram of half-subtractor incorporated with sleep transistor

5. SIMULATION AND RESULT

The simulation result of all the circuit has been placed. Half-subtractor circuit has been implemented. Transient response of the circuit is taken. Transient response is taken due the analyses the input and output response with power analysis.

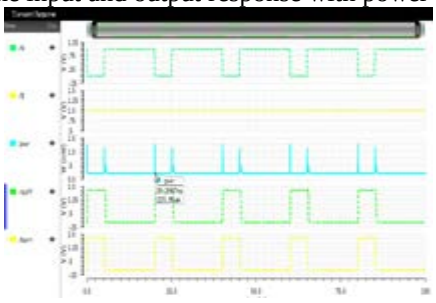

Figure 9: Output waveform of conventional half-subtractor

In conventional half-subtractor circuit which is operated in 1.8 v. To implement the half-subtractor circuit the AVLG and AVLS circuits where implemented. The reduction in the power consumption by incorporated with AVL Technique that is either AVLG or AVLS Technique.

The half-subtractor is created using the AVL technique and the power analysis is estimated where the power consumption is reduced in AVLS while compared with conventional half-subtractor.. On design-ing AVLS technique based Half-Subtractor using 180nmtechnology, we obtain a very low power consumption, less propagation delay.

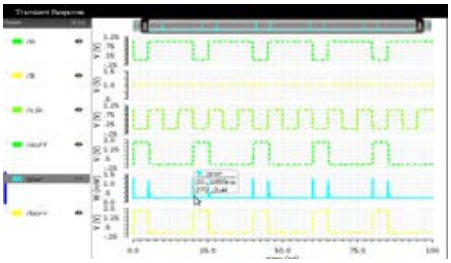

Figure 10:Output waveform of half-subtractor incorporated with AVLG

Here the simulation output shows that the power consumption will be reduced lightly when compared with conventional half-subtractor simulation result. Half-subtractor incorporated with AVLS circuit has a power consumption and propagation delay which is less than the half-subtractor incorporated with AVLG circuit.

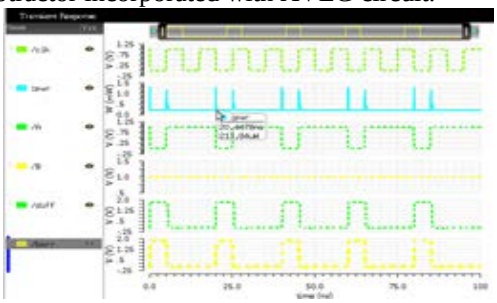

Figure 11: Output waveform of half-subtractor incorporated with AVLS

The power consumption of power gating circuitry is mainly consumed by the sleep transistor .

By applying an AVL with sleep transistor can have resultant power consumption and delay compared to AVLS technique ,the below diagram shows the half sub-tractor AVL with sleep transistor .

The ouput waveform of the half subtrac-tor incorporated with sleep transistor can have significant reduction in power and delay

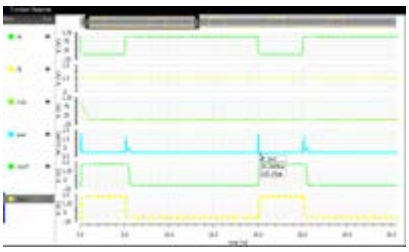

Figure 12:output waveform of half sub-tractor incorporated with sleep transistor

The comparison for the half-subtractor incorporated with AVLG circuit and AVLS circuit and half subtractor with sleep transistor technique are shown in a table.

TABLE2: COMPARISON OF POWER AND DELAY

Circuit Types	Power	Delay
Conventional HA sub	2.24E+02	4.70E-09
HA sub with AVLG	2.72E+02	4.69E-09
HA sub with AVLS	2.14E+02	4.45E-09
HA sub with sleep trans	2.02E+02	5.31E-11

The comparison results are shown in the form of graphical view. Here the power consumption is less in half subtractor with sleep transistor circuit while comparing with other two circuits (ie) AVLG circuit and AVLS circuit.

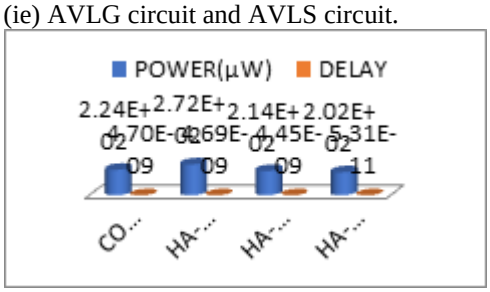

Figure 13: Graph for power and delay

6. CONCLUSION

Half-subtractor circuit is implemented using AVL with sleep transistor technique. These techniques were employed to reduce the power consumption and propagation delay. The design was implemented in Cadence virtuoso TMSC 180nm CMOS technology and it's obtain-ing the total power consumption 2.02E+02ns and delay 5.31E-11 . The requirements of energy optimized low power a circuit is used in higher end applications such as communication, IoT, biomedical systems etc., The entire circuit is operating at 1.8V. Everything has been done in the cadence. This tool it is easy to analysis output of the circuit.

REFERENCES

[1] ShyamAkashe, Gunakesh Sharma, RichaPandey, VinodRajak "Implementa-tion of high performance and low leakage half subtractor circuit using AVL tech-nique"978-1-4673-4805-8/12/$31.00_c2012 IEEE.

[2] TanviSood, Rajesh Mehra" Design a Low Power Half-Subtractor Using .90µm CMOS Technology" Volume 2, issue 3 (May. –Jun. 2013), PP 51-56 e-ISSN: 2319 4200, p-ISSN No. : 2319 –4197.

[3] MilindGautam, ShyamAkashe "Re-duction of Leakage Current and Power in Full-Subtractor Using MTCMOS Tech-nique" 978-1-4673-2907-1/13/$31.00 ©2013 IEEE.

[4] H.Mangalam and K.Gunavathi "Gate and subthreshold leakage reduced SRAM cells" DSP Journal, Volume 6, Issue 1, September, 2006.

[5] B. Dilli Kumar1, M. Bharathi2 " De-sign and analysis of adiabatic full subtrac-tor for low powerapplications" Issue 3 volume 1, January-February 2013ISSN 2249-9954.

[6] R. K. Singh, Neeraj Kr. Shukla, and Manisha Pattanaik, "Characterization of a Novel Low-Power SRAM Bit-Cell Struc-ture at Deep Sub-Micron CMOS technology for Multimedia Applications," Circuit and Systems, USA, Vol.3 No.1, Jan. 2012.

[7] V. De and S. Borkar,"Technology and design challenges for low power and high performance," in Proc. Int. Symp. Low Power Electronics and Design, 1999, pp. 163-168. (Pubitemid) 30502858.

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